In some embodiments of the present disclosure, the method further includes forming an epitaxy region in proximity to the upper width of the metal gate.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A semiconductor structure, comprising:

a substrate having a center portion and an edge portion;

a plurality of semiconductor dies over the substrate, the edge portion including a region where at least one side of the semiconductor die being in contact with the circumference of the substrate;

an isolation layer over the plurality of semiconductor dies;

a semiconductor fin with a top surface and a sidewall surface, partially positioning in the isolation layer;

a first gate covering a portion of the top surface and a portion of the sidewall surface of the semiconductor fin, positioning at the edge portion of the substrate; and

a second gate covering a portion of the top surface and a portion of the sidewall surface of the semiconductor fin, positioning at the center portion of the substrate,

wherein a lower width of the first gate in proximity to the isolation layer is smaller than an upper width of the first gate in proximity to top surface of the semiconductor fin.

2. The semiconductor structure of claim **1**, wherein the substrate further comprises a dense gate region and an isolated gate region at the center portion and at the edge portion of the substrate.

3. The semiconductor structure of claim **1**, a difference between the lower width and the upper width is below 15 nm.

4. The semiconductor structure of claim **3**, a 3-sigma value of the difference between the lower width and the upper width measured by a spectroscopic critical dimension method is below about 2 nm.

5. The semiconductor structure of claim **3**, a range of the difference between the lower width and the upper width measured by a spectroscopic critical dimension method is below about 2.6 nm.

6. The semiconductor structure of claim **2**, a difference between the lower width and the upper width of the second gate in the isolated gate region minus a difference between the lower width and the upper width of the first gate in the isolated gate region is less than about 2.5 nm.

7. The semiconductor structure of claim **2**, a difference between the lower width and the upper width of the second gate in the dense gate region and a difference between the lower width and the upper width of the first gate in the dense gate region is substantially identical.

8. A FinFET structure, comprising:

a first semiconductor fin having a top surface and a sidewall surface;

a first metal gate over a portion of the first semiconductor fin, surrounding the top surface and the sidewall surface of the first semiconductor fin, the first metal gate being positioned on a semiconductor die at an edge portion of a substrate the edge portion including a region where at least one side of the semiconductor die being in contact with the circumference of the substrate;

wherein a first metal gate width at a bottom of the first metal gate is smaller than a second metal gate width at the top surface of the first semiconductor fin.

9. The FinFET structure of claim **8**, wherein a difference between the first metal gate width and the second metal gate width is below 15 nm.

10. The FinFET structure of claim **9**, wherein the second metal gate width is in a range of from about 28 nm to about 32 nm.

11. The FinFET structure of claim **9**, wherein the second metal gate width is in a range of from about 235 nm to about 245 nm.

12. The FinFET structure of claim **10**, a difference between the first metal gate width and the second metal gate width is in a range of from about 1.5 nm to about 2.5 nm.

13. The FinFET structure of claim **11**, further comprising a second metal gate over a portion of a second semiconductor fin, surrounding the top surface and the sidewall surface of the second semiconductor fin, the second metal gate being positioned on a semiconductor die at a center portion of the substrate, wherein a third metal gate width at a bottom of the second metal gate is smaller than a fourth metal gate width at the top surface of the second semiconductor fin; and

a ratio of a difference between the first metal gate width and the second metal gate width at an edge portion of a substrate and a difference between the third metal gate width and the fourth metal gate width at the center portion of the substrate is below about 2.

14. The FinFET structure of claim **10**, further comprising a second metal gate over a portion of a second semiconductor fin, surrounding the top surface and the sidewall surface of the second semiconductor fin, the second metal gate being positioned on a semiconductor die at a center portion of the substrate, wherein a third metal gate width at a bottom of the second metal gate is smaller than a fourth metal gate width at the top surface of the second semiconductor fin; and

a difference between the first metal gate width and the second metal gate width at the edge portion of a substrate and a difference between the third metal gate width and the fourth metal gate width at the center portion of the substrate is substantially identical.

15. A FinFET structure, comprising:

a semiconductor fin having a top surface and a sidewall surface; and

a first gate covering a portion of the top surface and a portion of the sidewall surface of the semiconductor fin, the first gate being positioned on a semiconductor die at an edge portion of the substrate, the edge portion including a region where at least one side of the semiconductor die being in contact with the circumference of the substrate;

wherein a lower width of the first gate in proximity to a bottom of the sidewall surface is smaller than an upper width of the first gate in proximity to the top surface of the semiconductor fin.

16. The FinFET structure of claim **15**, further comprising a second gate covering a portion of the top surface and a portion of the sidewall surface of the semiconductor fin, wherein a lower width of the second gate in proximity to the bottom of the sidewall surface is smaller than an upper width of the second gate in proximity to the top surface of the semiconductor fin.